

FIG.1

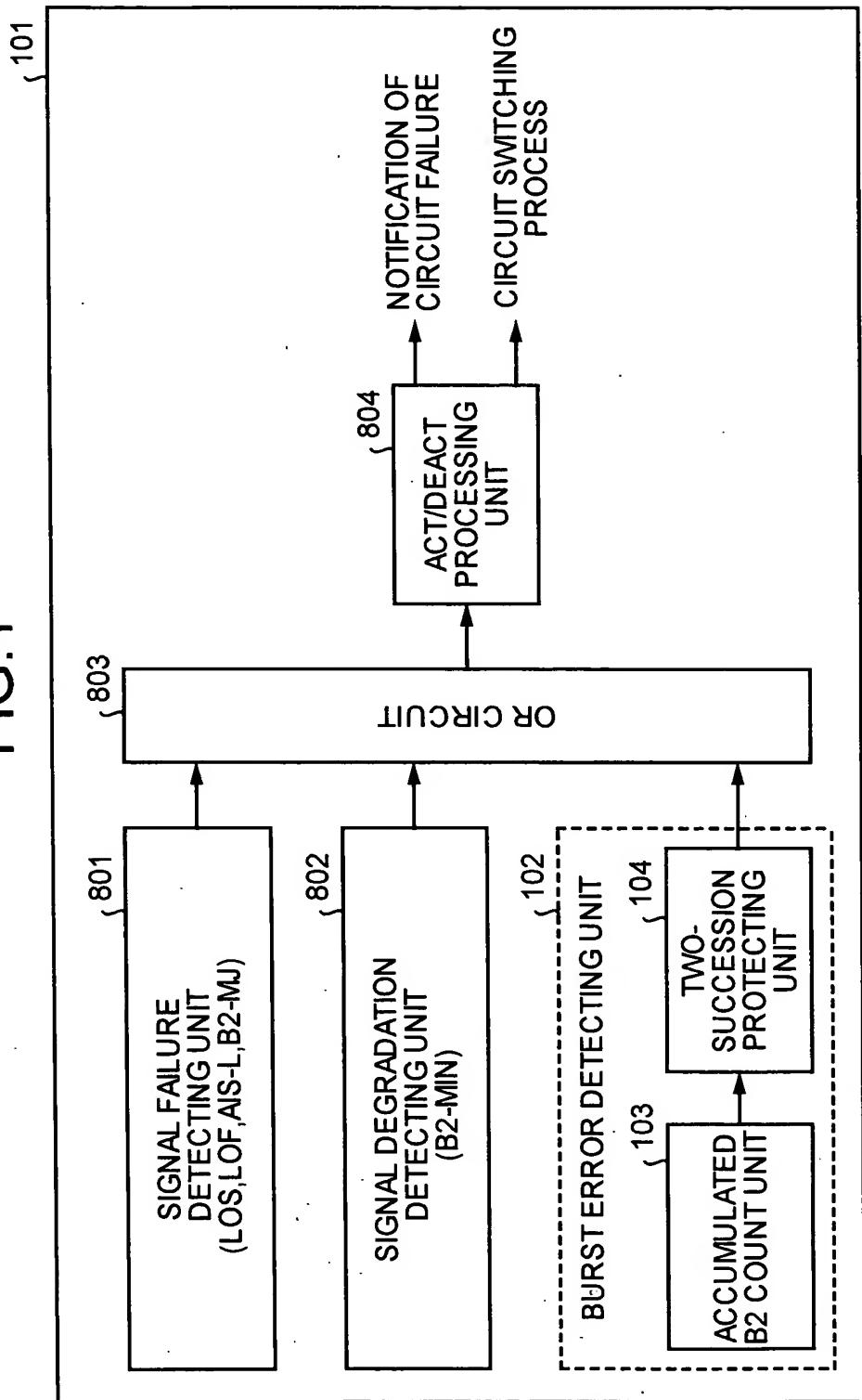


FIG.2

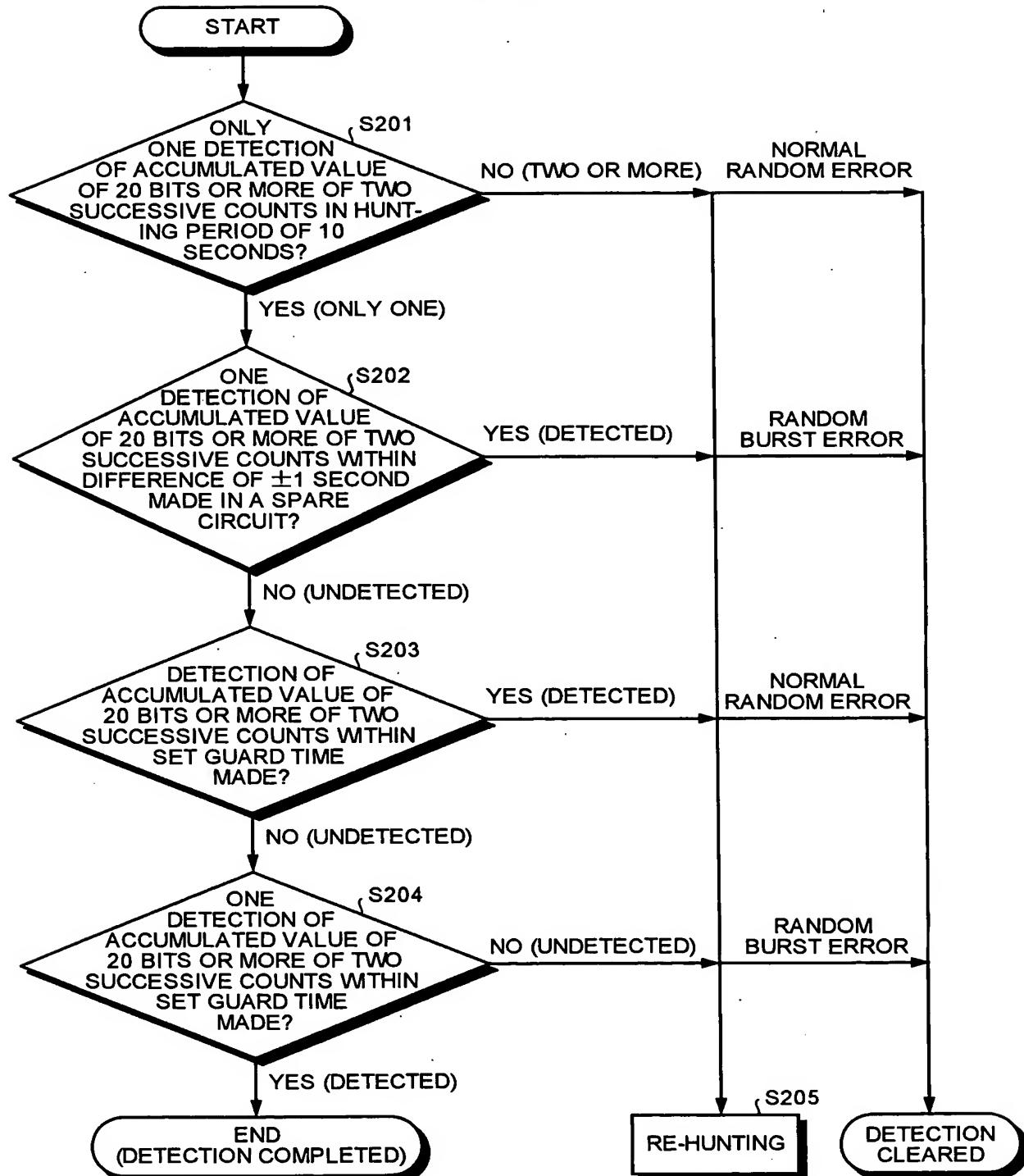


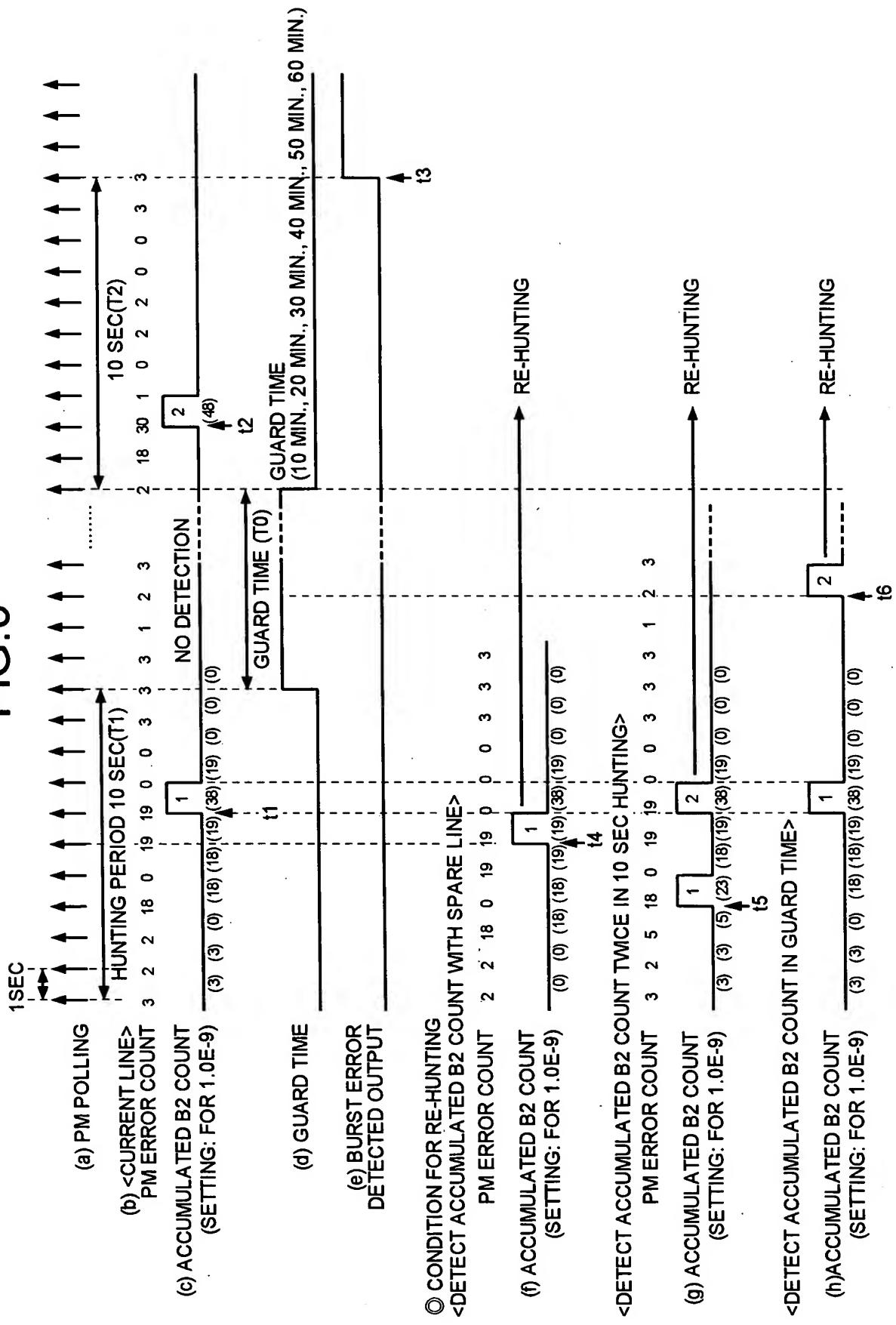
FIG. 3

FIG. 4

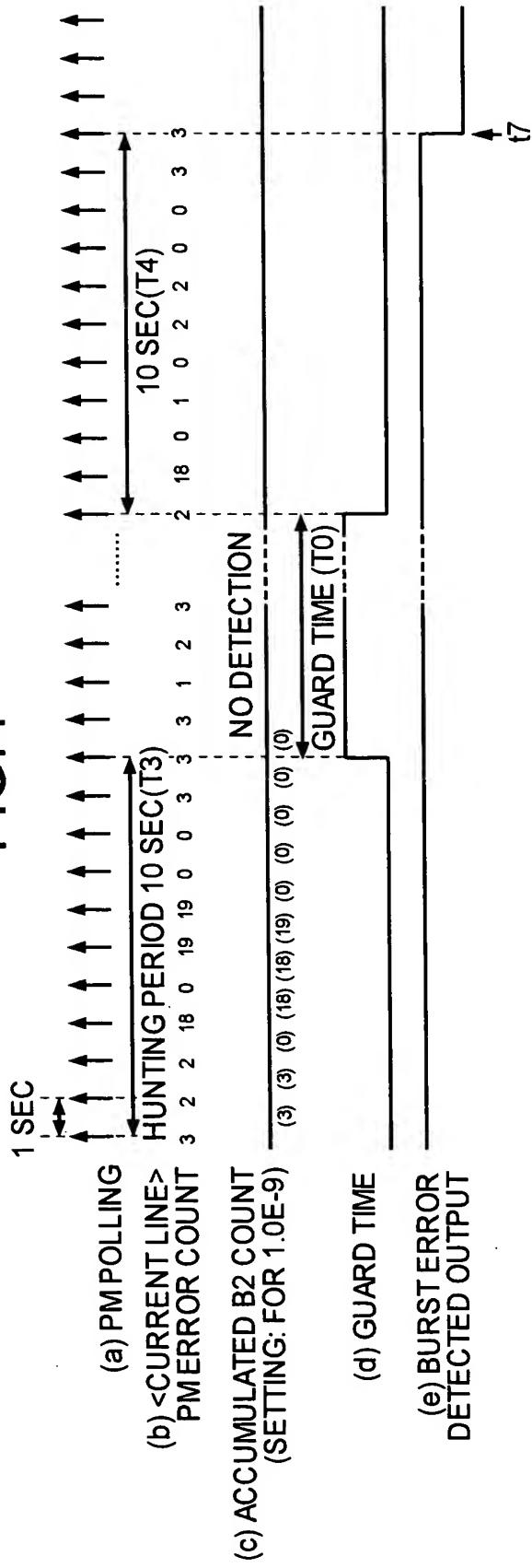


FIG.5

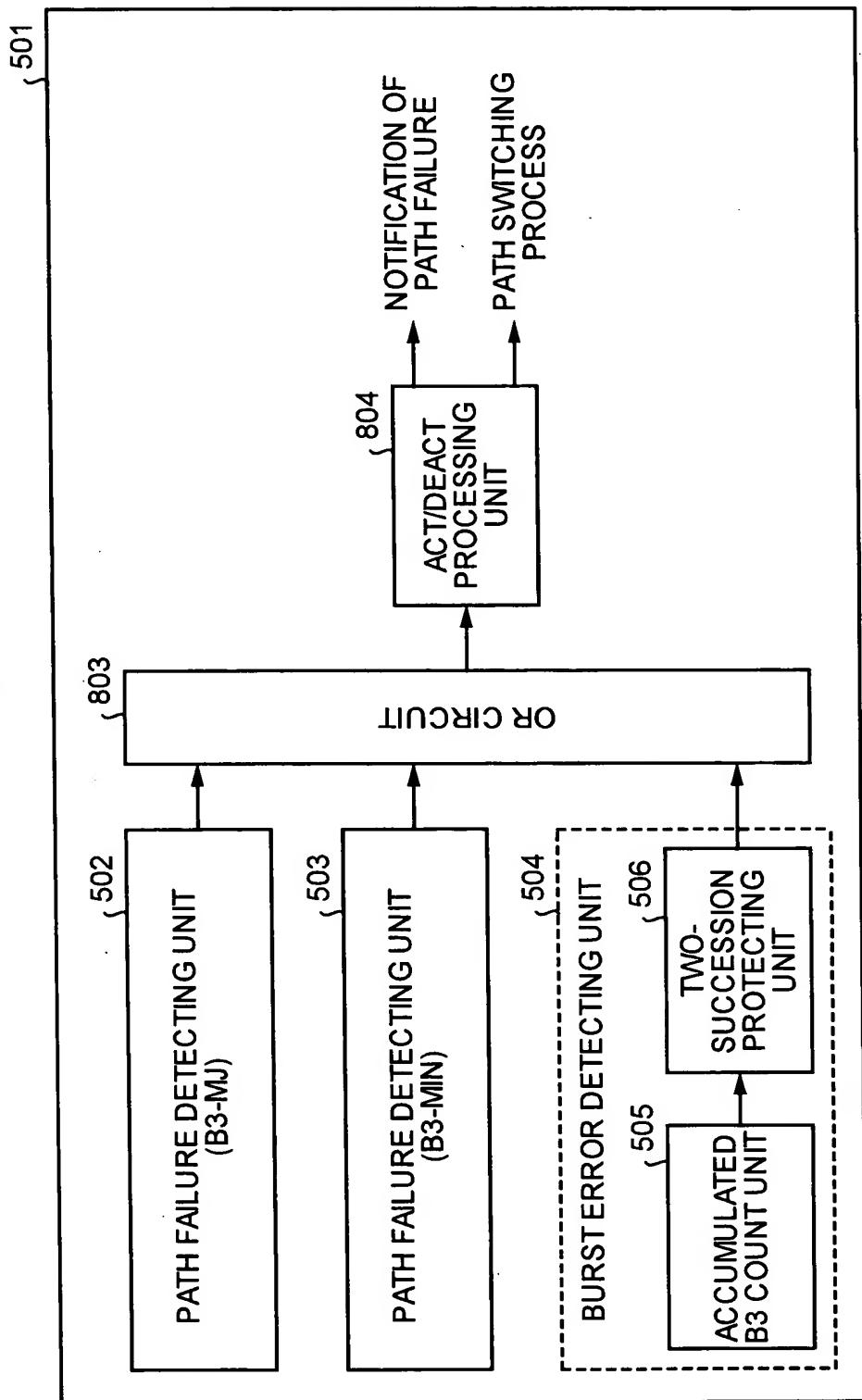


FIG. 6A

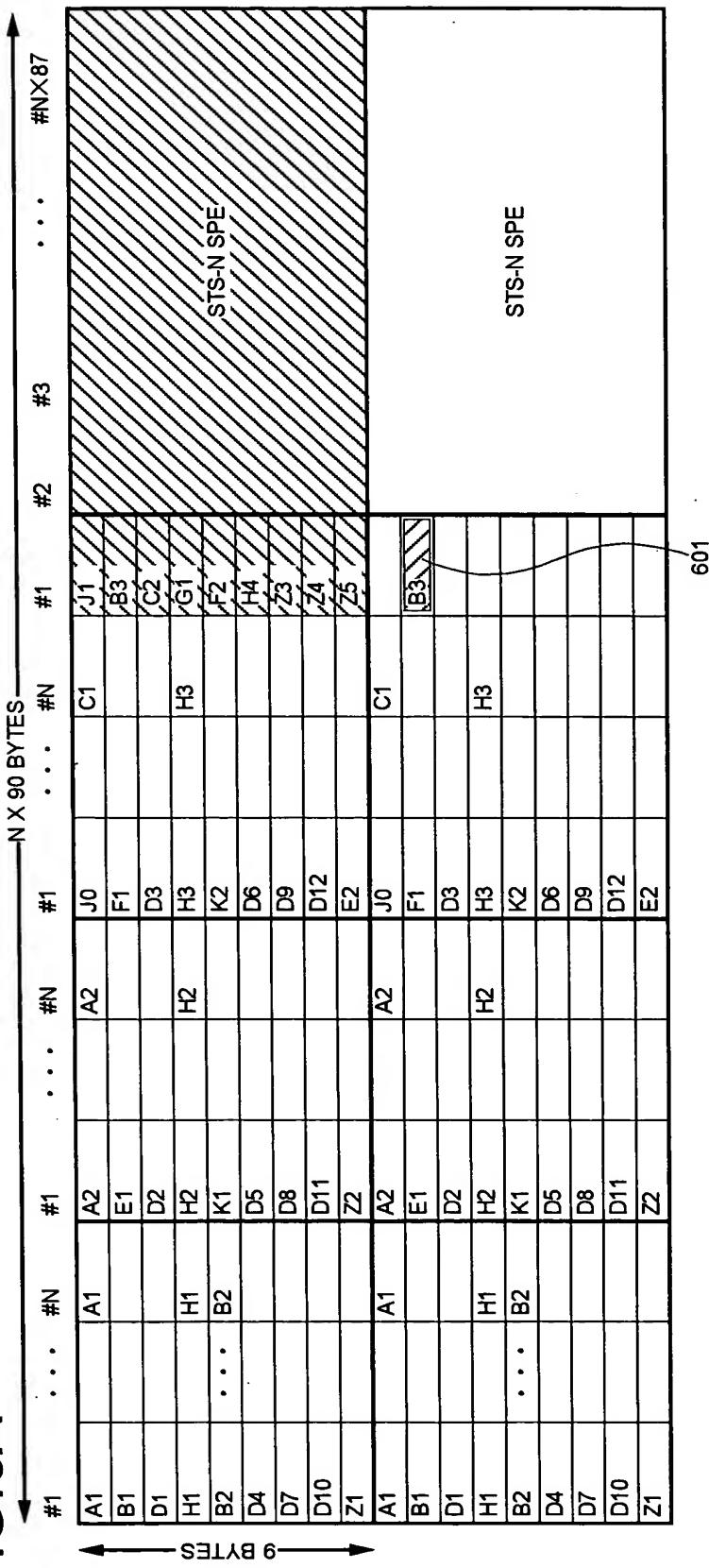


FIG. 6B

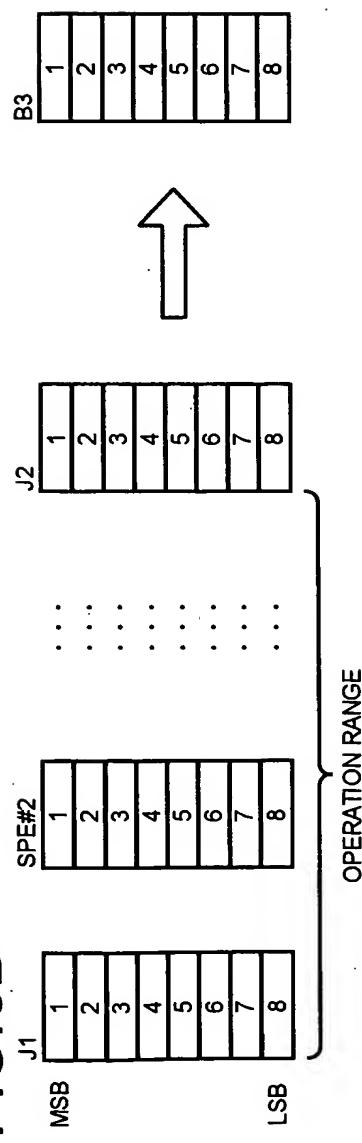


FIG.7

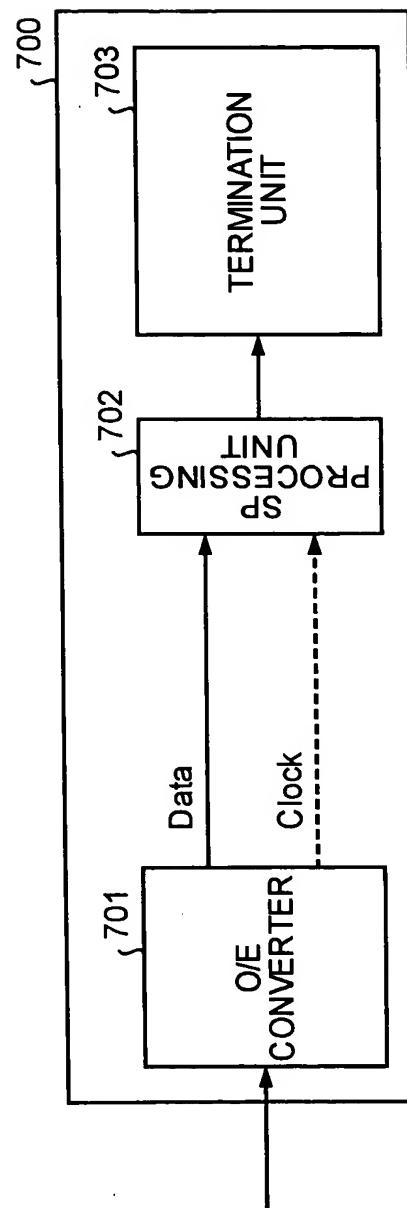


FIG.8

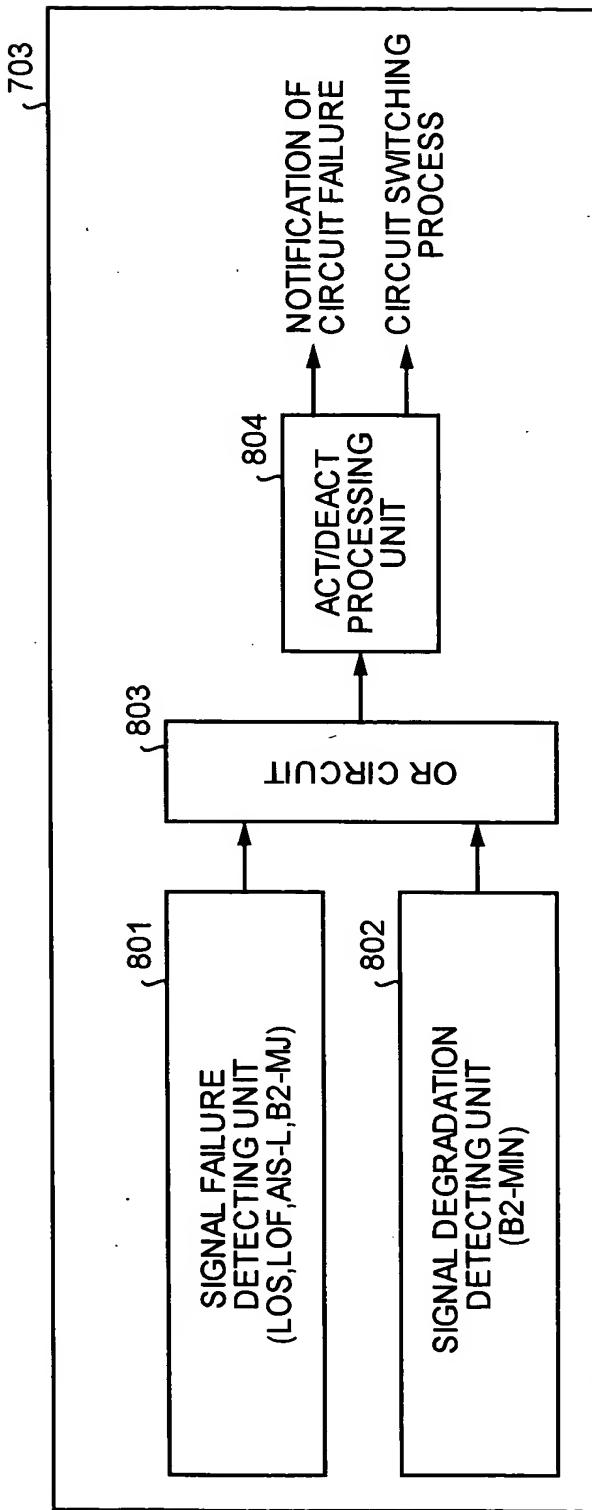
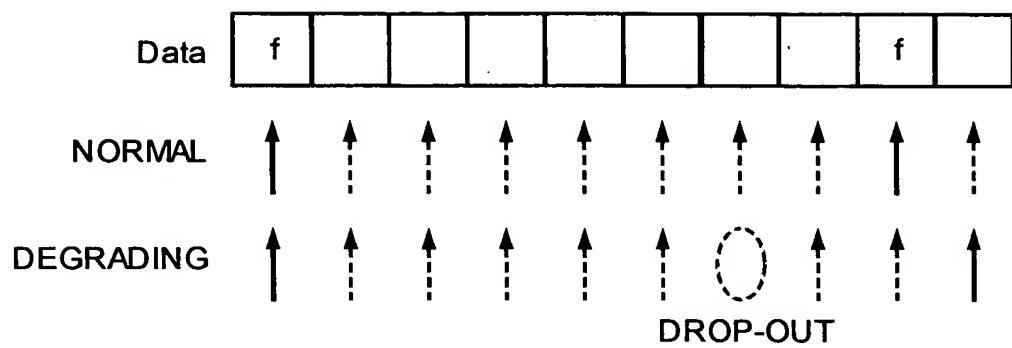
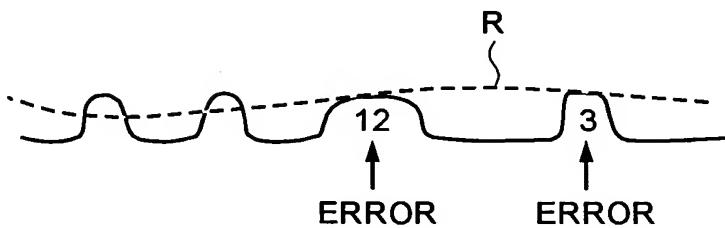


FIG.9A**FIG.9B**

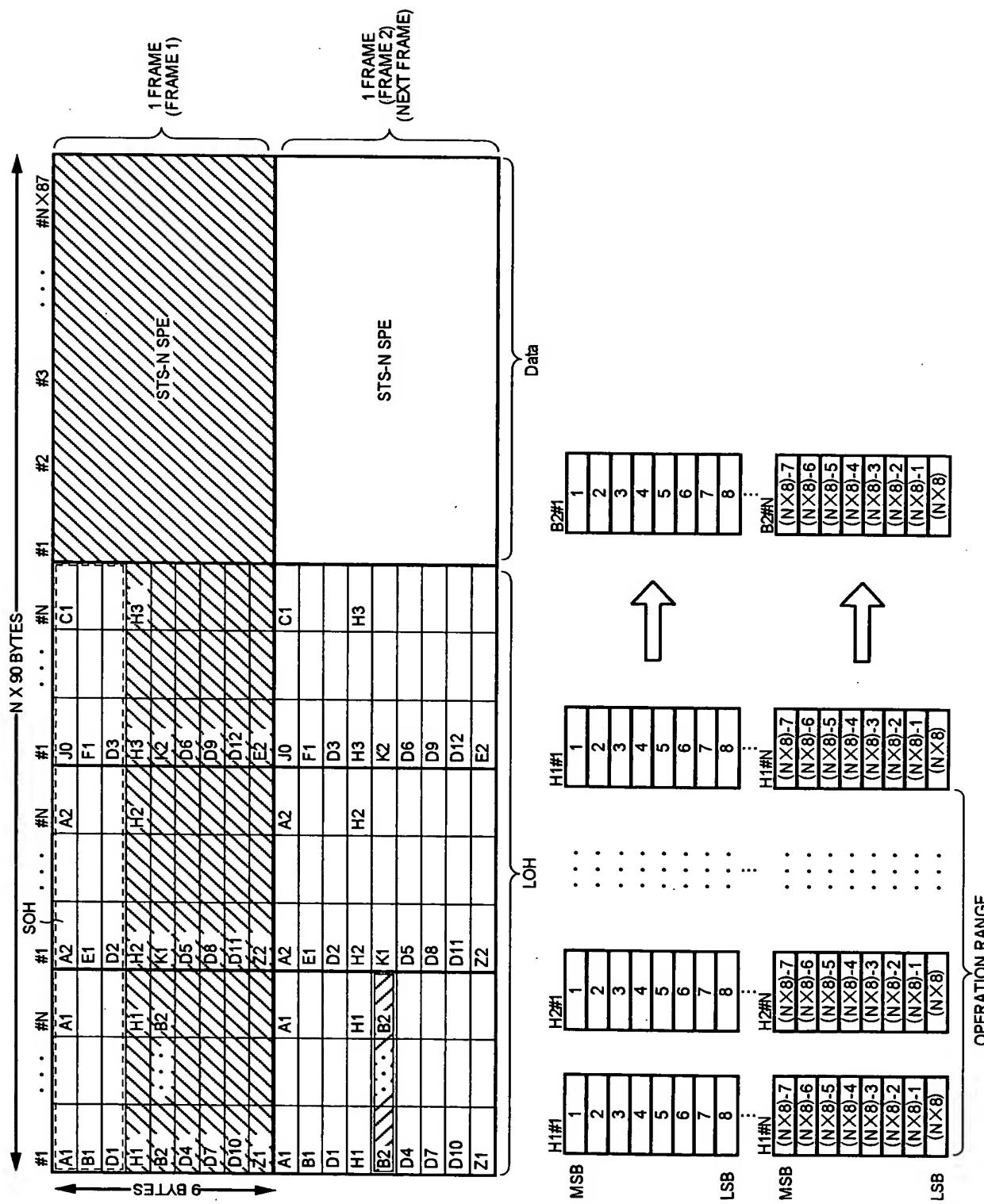


FIG. 10A

FIG.11

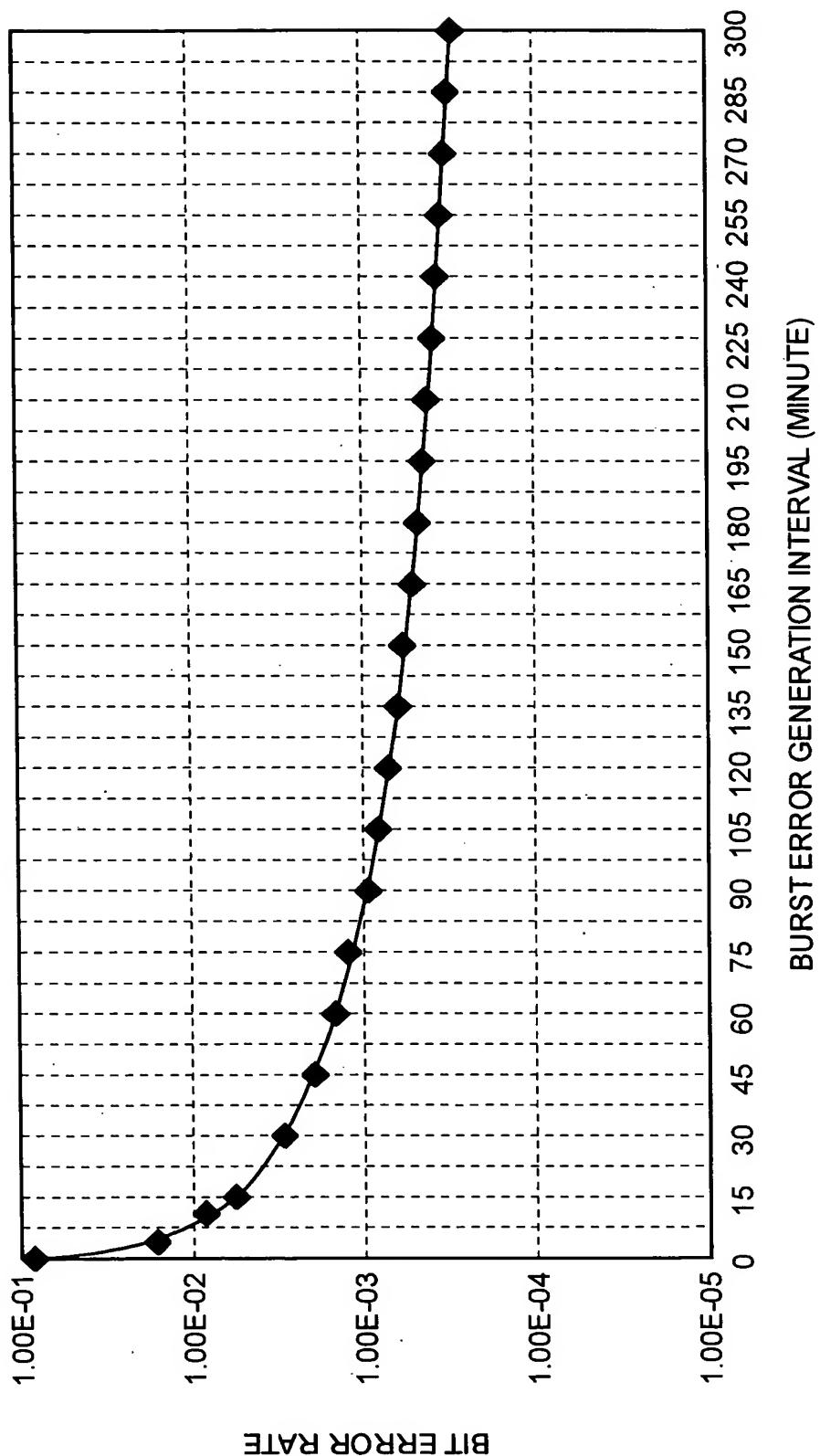


FIG. 12

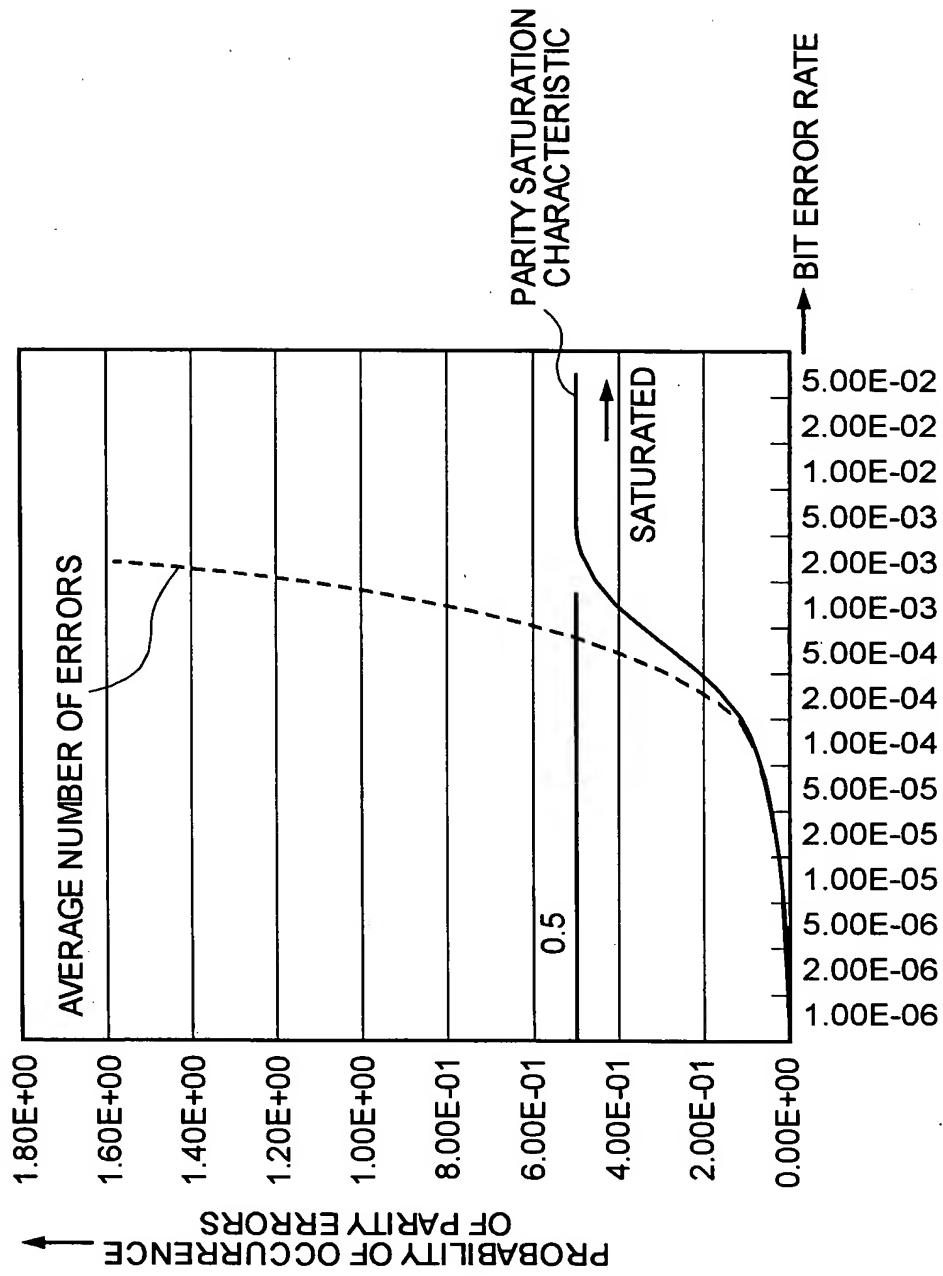


FIG. 13

BIT ERROR RATE	DETECTION CIRCUIT STANDARDS					THEORETICAL VALUE			
	MONITOR FRAME LENGTH	MONITOR TIME (SEC)	NUMBER OF SUCCES- SIONS	DETEC- TION TIME (SEC)	NUMBER OF DETEC- TED ERRORS				
1.0E-03	1	0.00013	150	58	0.00725	8700	1,200,000	4.88E-04	2,460,672
1.0E-04	9	0.00113	204	7	0.00788	1428	181,333	7.37E-05	246,067
1.0E-05	90	0.01125	204	7	0.07875	1428	18,133	7.37E-06	24,607
1.0E-06	900	0.11250	204	7	0.78750	1428	1,813	7.37E-07	2,461
1.0E-07	9,000	1.12500	204	7	7.87500	1428	181	7.37E-08	246
1.0E-08	90,000	11.25000	204	7	78.75000	1428	18	7.37E-09	25
1.0E-09	900,000	112.50000	204	7	787.50000	1428	2	7.37E-10	2